Amendments to the Abstract:

Please add the following Abstract:

An area-efficient realization of a coefficient block includes hardware sharing techniques and optimizations applied to this block. The block is connected to coefficient lines coming from a delay block to be connected to perform a filtering operation or a mathematical computing operation with optimization in hardware and provides a zero latency output. The coefficient block also enables an area minimal realization of digital filters based on the coefficient block, when operated in serial bit fashion. The optimization techniques and structure are good for bit-serial digital filters typically a finite impulse response (FIR) filter, including finite impulse response filter (IIR) and for other filters and applications based on combinational logic that includes delay elements, multipliers, and serial adders and/or subtractors.